数字系统设计作业

**学号： 519021911101 姓名： 颜琪滨 日期： 2021/12/08**

**第1题：**

**（1）设计模块**

**（2）测试模块**

**（3）测试波形图：如果很多，可以提供部分波形内容；**

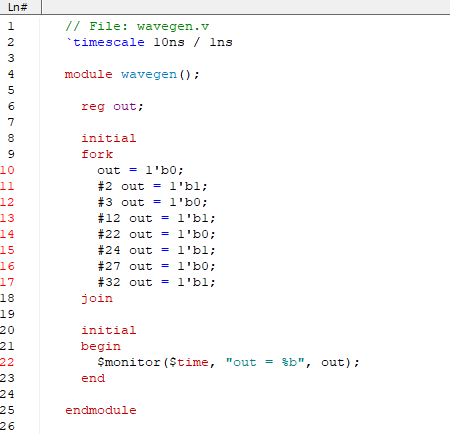
**（4）显示输出（可选）：如果需要显示输出来说明模块设计的正确性；**

**（5）设计说明（可选）：如果有需要说明的部分。**

**第1题：**

1. **设计模块**

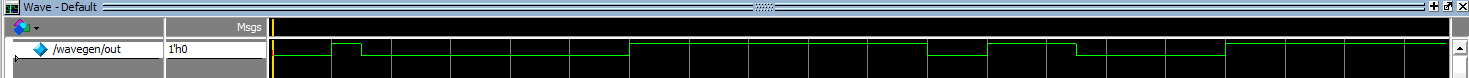
**根据图上的时间依次赋值即可。**



1. **测试模块**

**本题没有要求，因此空着了。**

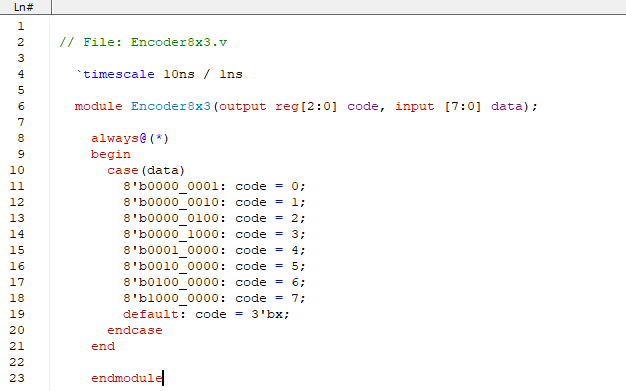
1. **测试波形图：**



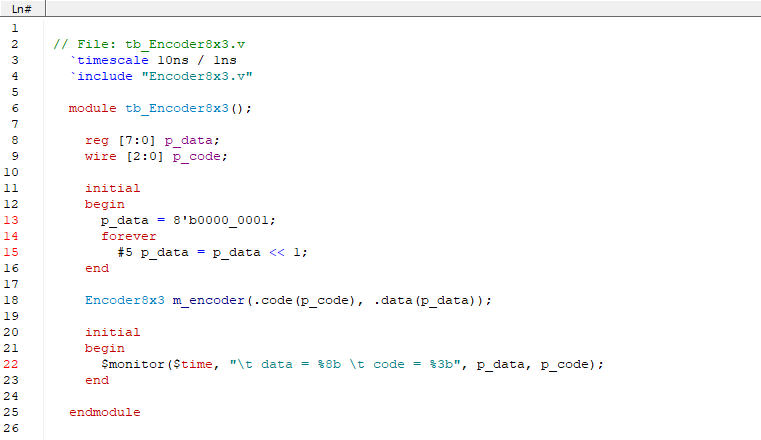
**第2题：**

1. **设计模块**

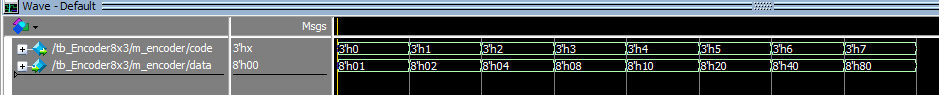
**按照编码器真值表构造即可。**



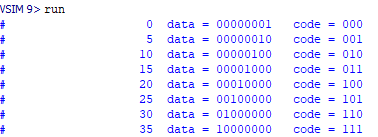
1. **测试模块**



1. **测试波形图：**

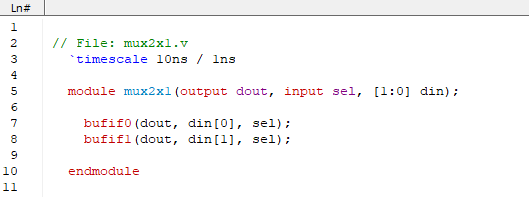


1. **显示输出（可选）：**

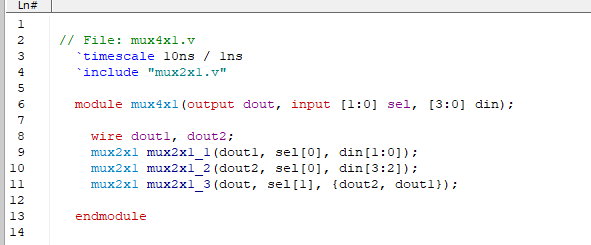


**第3题：**

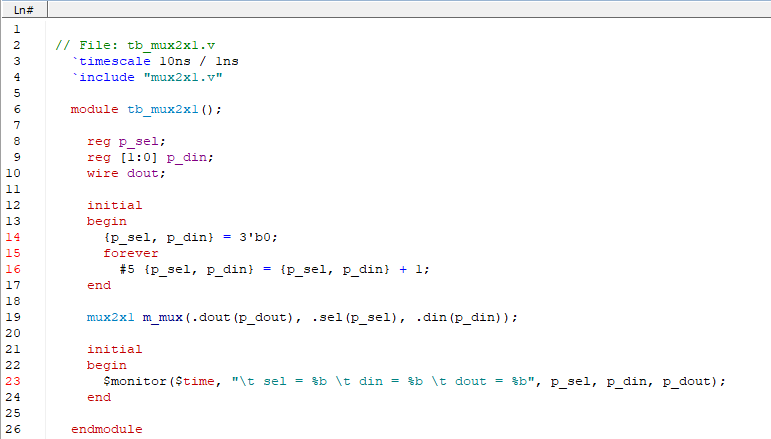
1. **设计模块**
2. **mux2x1.v**



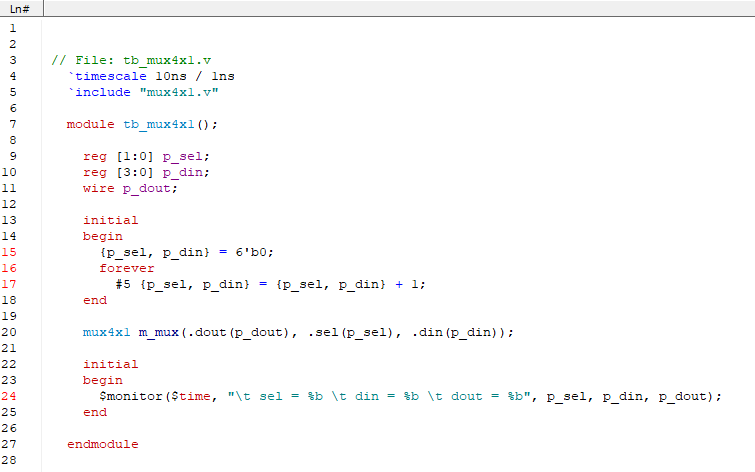
1. **mux4x1.v**



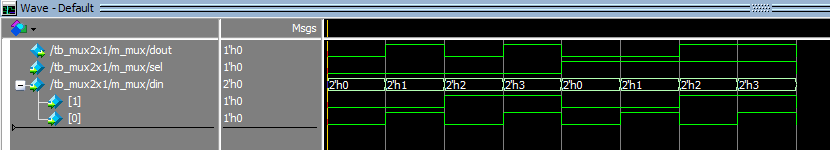
1. **测试模块**
2. **tb\_mux2x1.v**



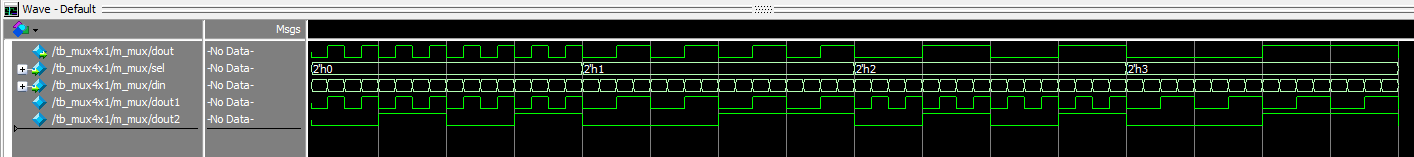
1. **tb\_mux4x1.v**



1. **测试波形图：**

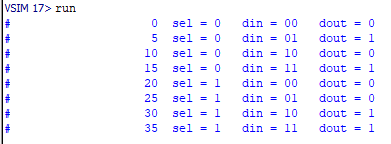
**(a)** 

**(b)**

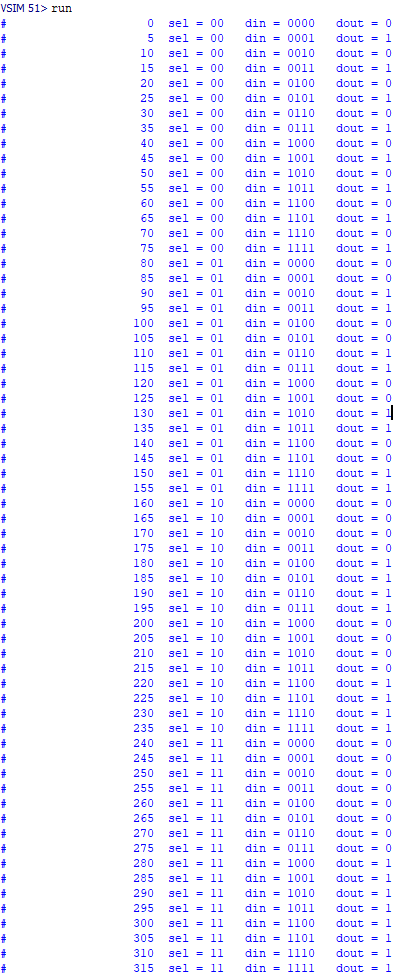


**（4）显示输出（可选）：**

**(a)**

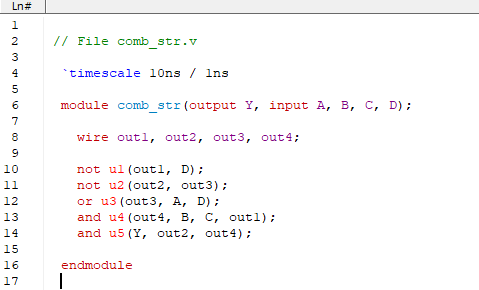


**(b)**

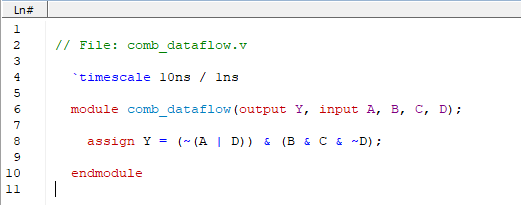


**第4题：**

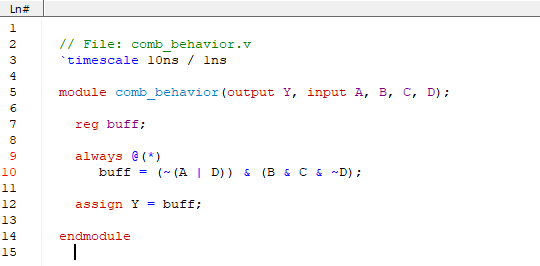
1. **设计模块**
2. **comb\_str.v**



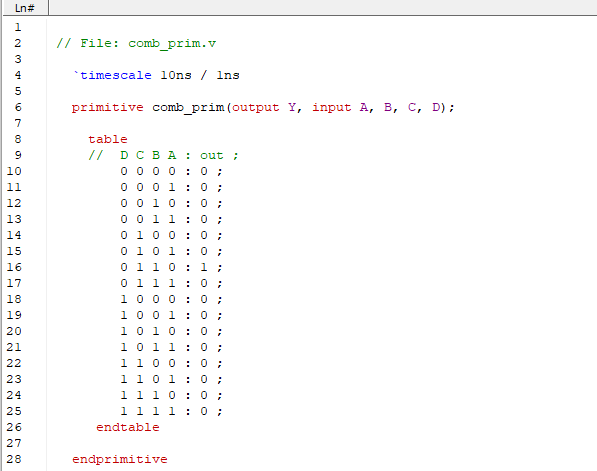
1. **comb\_dataflow.v**



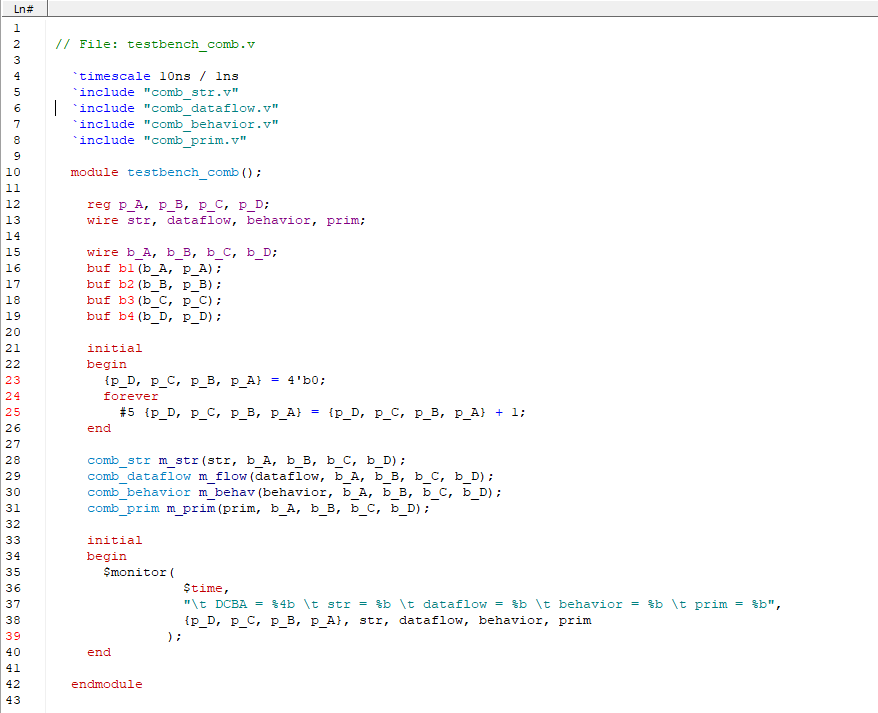
1. **comb\_behavior.v**



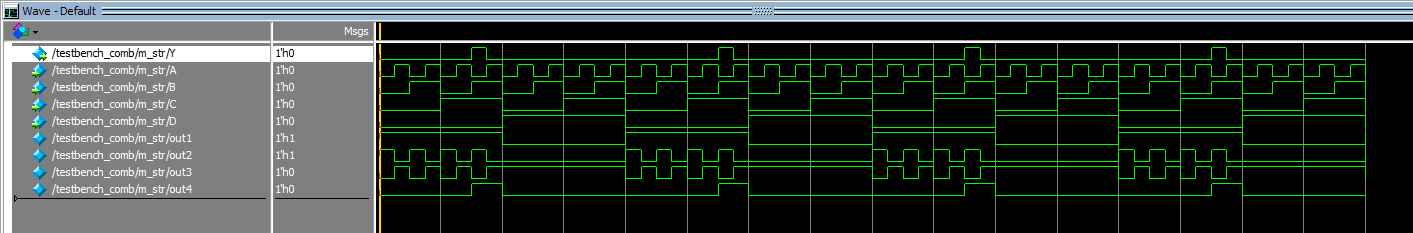
1. **comb\_prim.v**



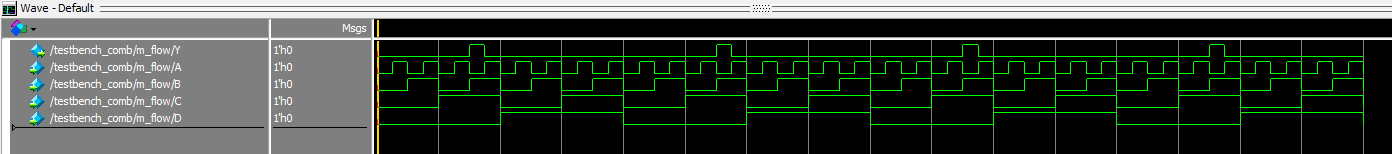
1. **测试模块**



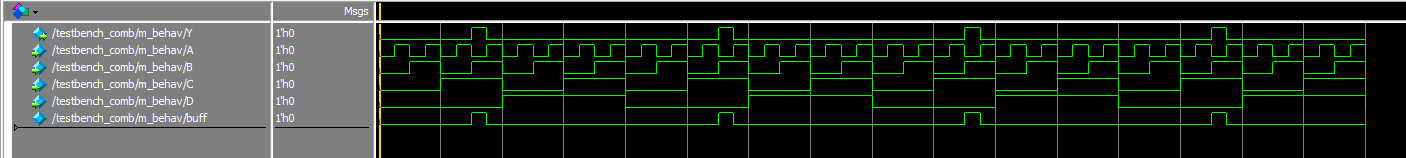
1. **测试波形图：**
2. **Str**



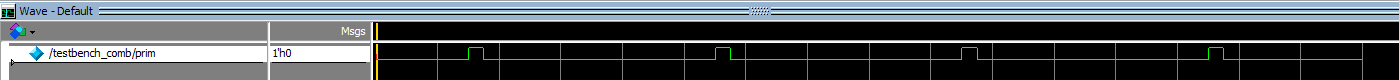
1. **Dataflow**



1. **Behavior**

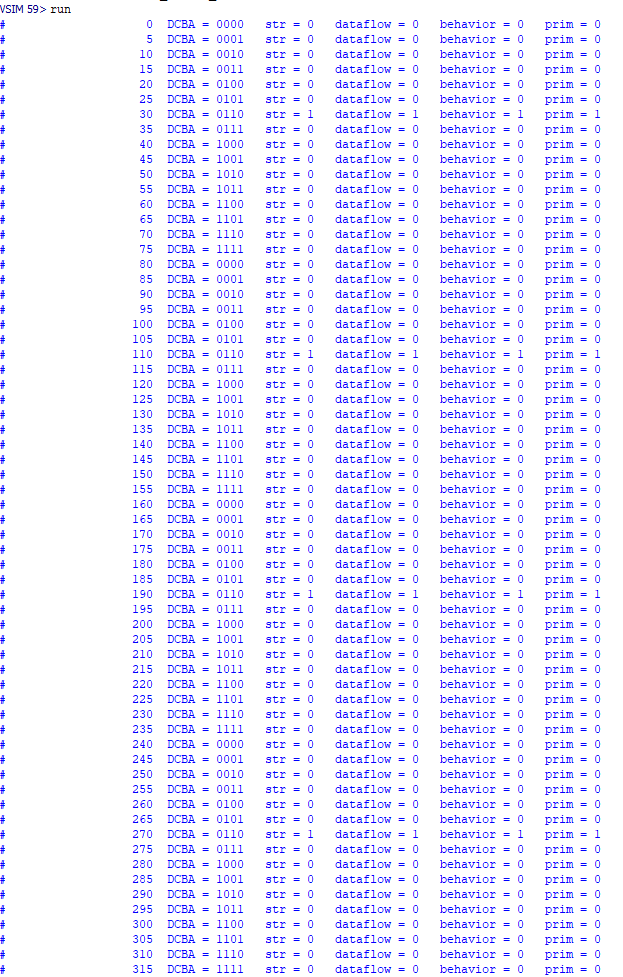


1. **Prim**



1. **显示输出（可选）：**

**使用$monitor监视仿真结果，并在Transcript Window中输出文本表示的仿真结果。**



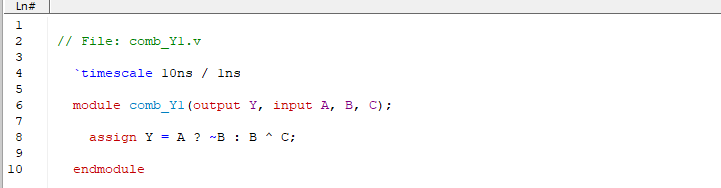
1. **设计说明（可选）：**

**在testbench\_comb.v中，分别对comb\_str, comb\_dataflow, comb\_behavior, comb\_prim进行测试，并将结果存在wire类型变量str, dataflow, behavior, prim中。此外，还用buf门缓存A,B,C,D的值。**

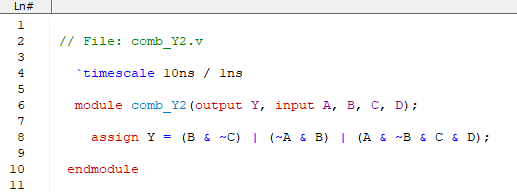
**第5题：**

1. **设计模块**

**(i)**

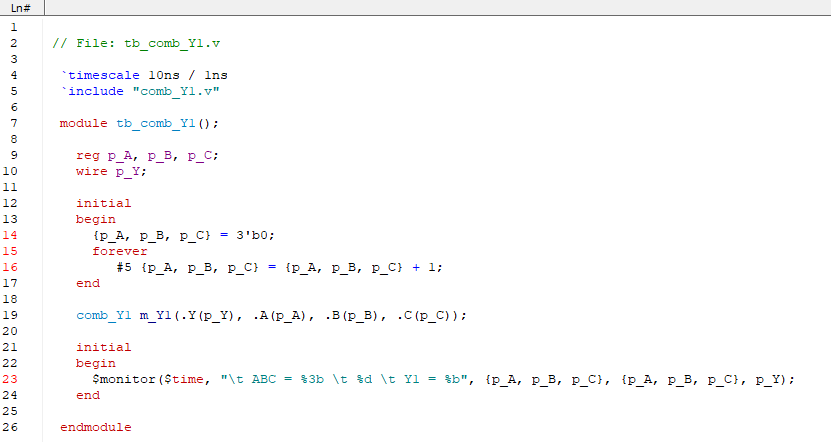


**(ii)**

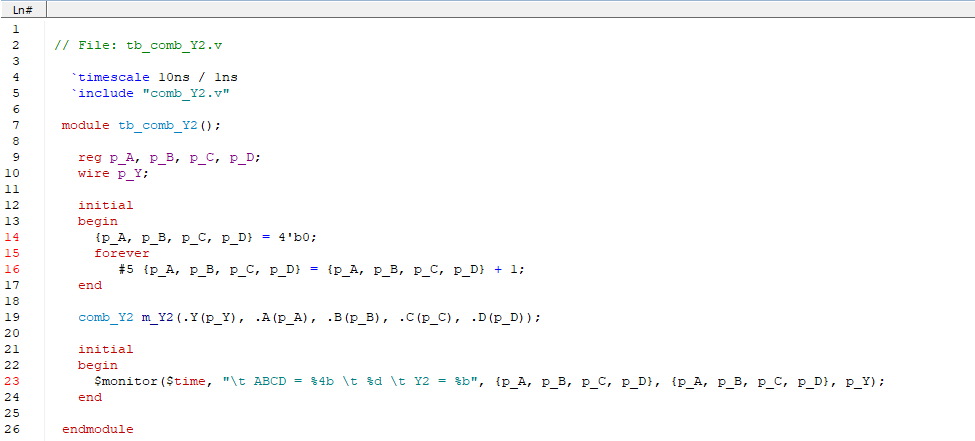


1. **测试模块**

**(i)**

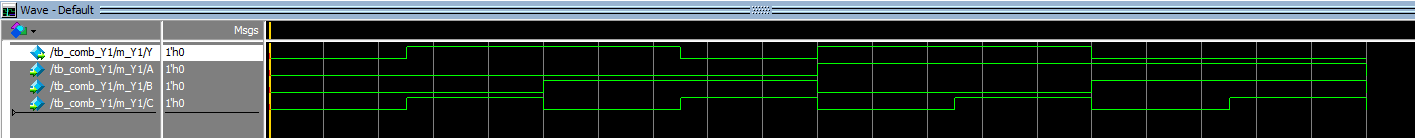


**(ii)**

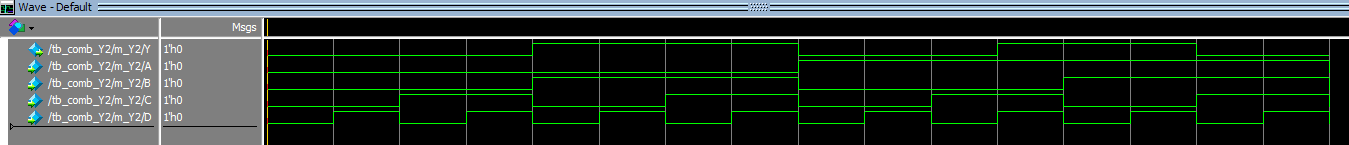


1. **测试波形图：**

**(i)**

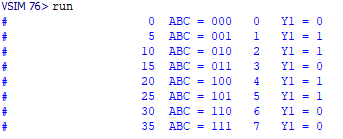


**(ii)**

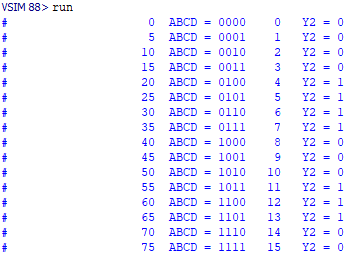


1. **显示输出：**

**(i)**



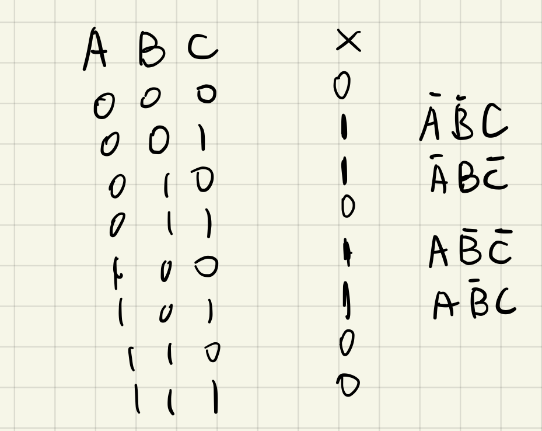
**(ii)**



1. **设计说明：**

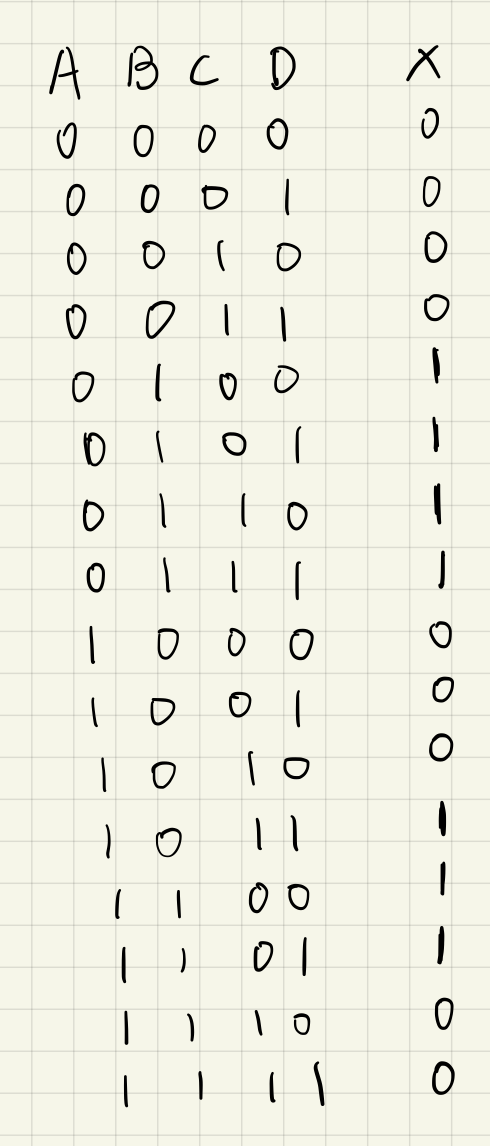
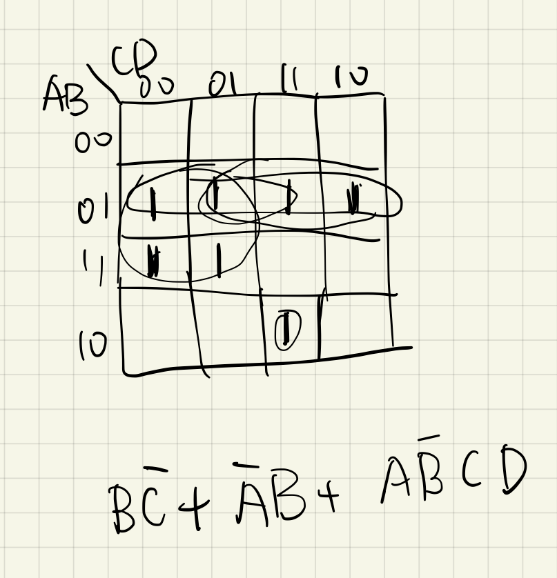
**(i)**

**题中的布尔方程是最小项之和的形式，画出其真值表，不难发现，输出可以表达为Y=A?~B:B^C。**

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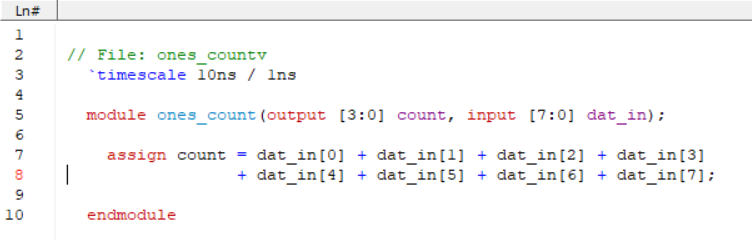
**(ii)**

**题中的布尔方程是最小项之和的形式，画出其真值表，画出卡诺图进行化简。结合起来即为：Y = (B & ~C) | (~A & B) | (A & ~B & C & D);**

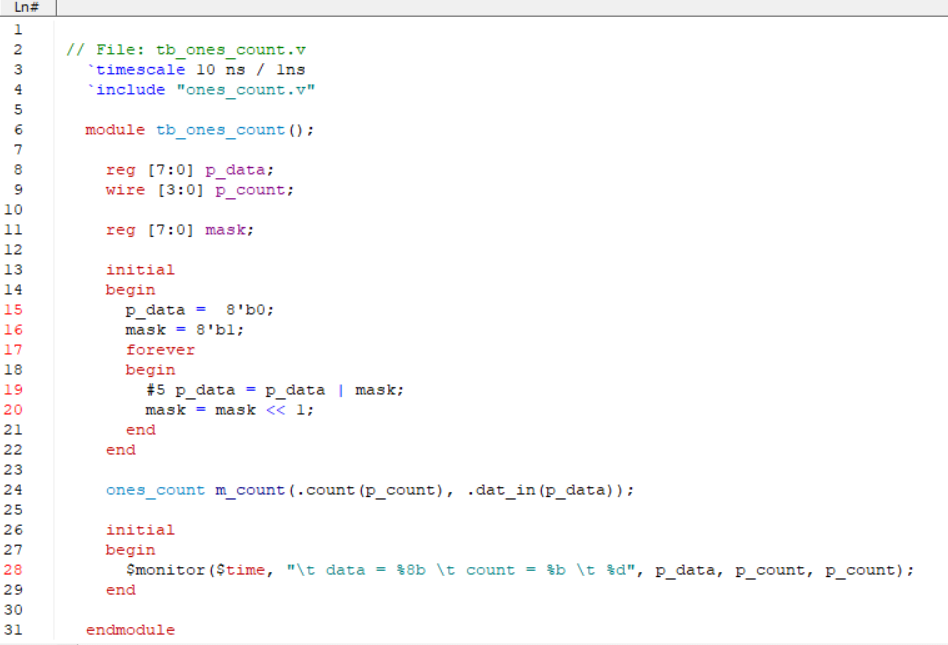
**** ****

**第6题：**

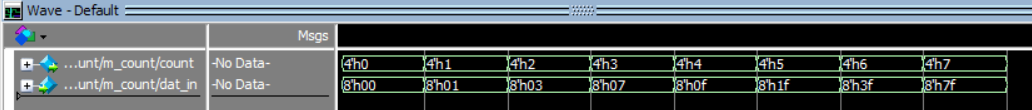
1. **设计模块**



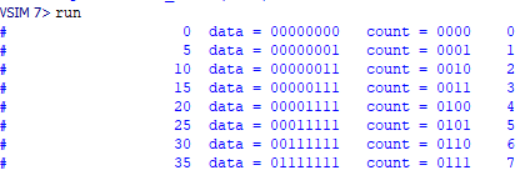
1. **测试模块**



1. **测试波形图：**

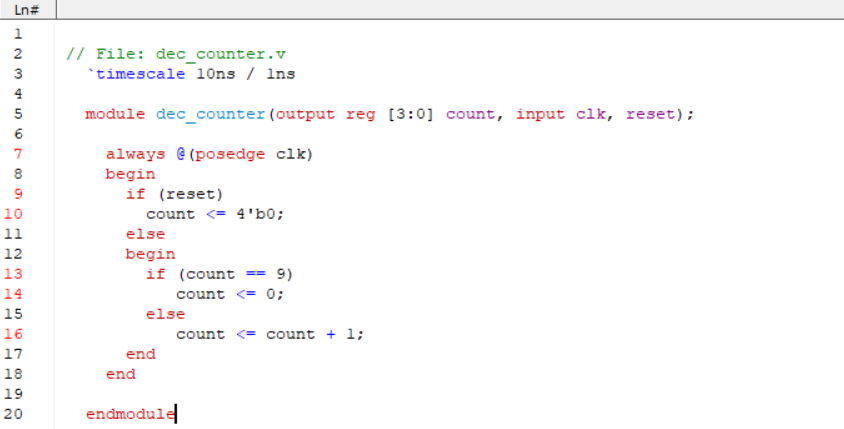


1. **显示输出：**

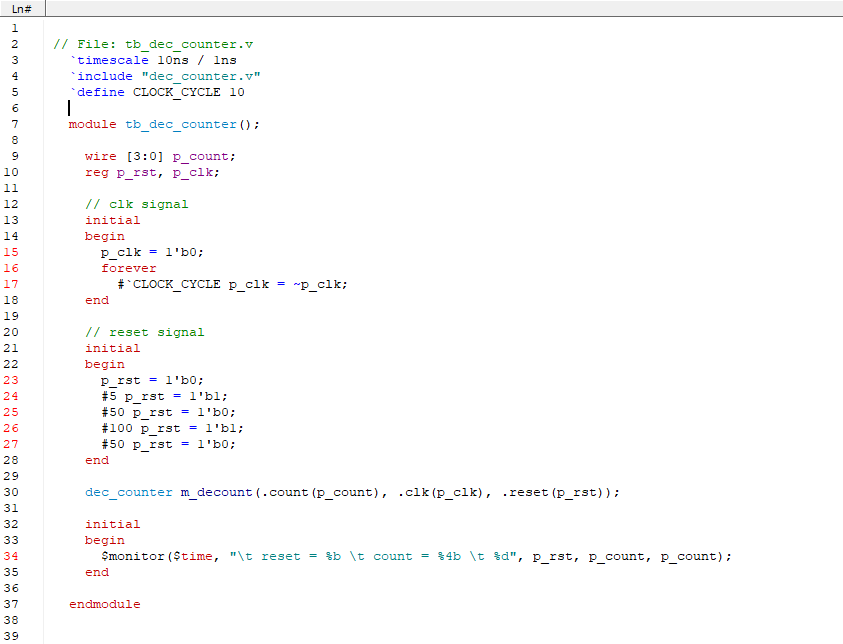


**第7题：**

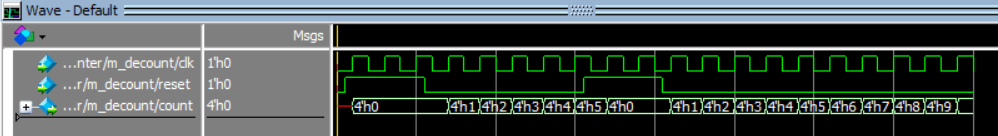
1. **设计模块**



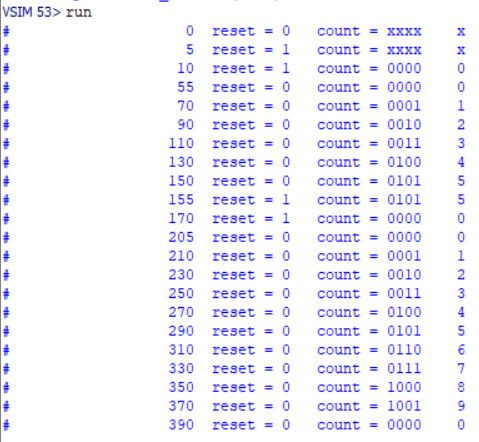
1. **测试模块**



1. **测试波形图：**

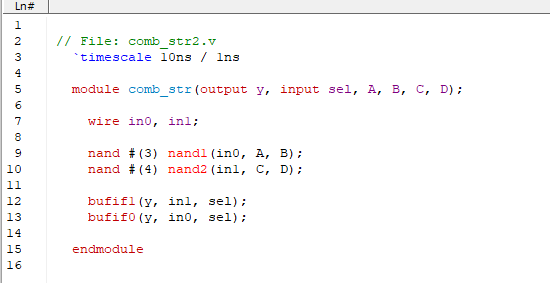


1. **显示输出：**

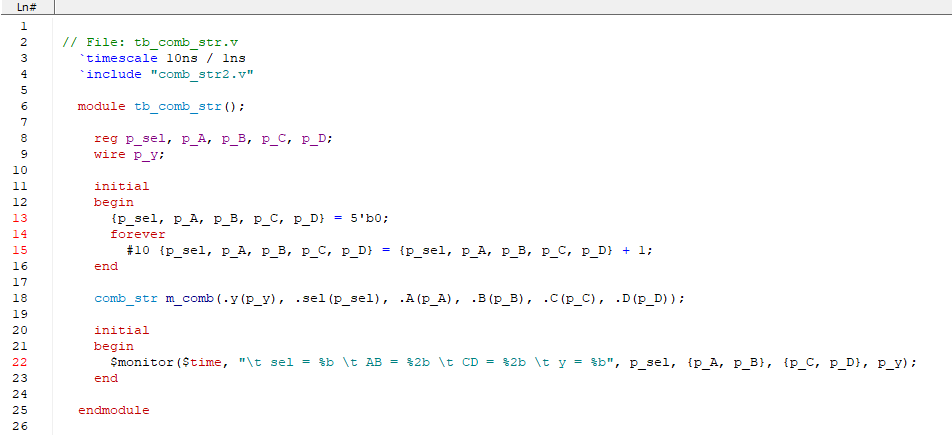


**第8题：**

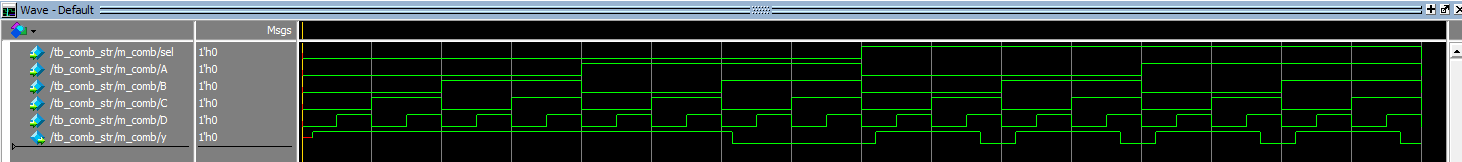
1. **设计模块**



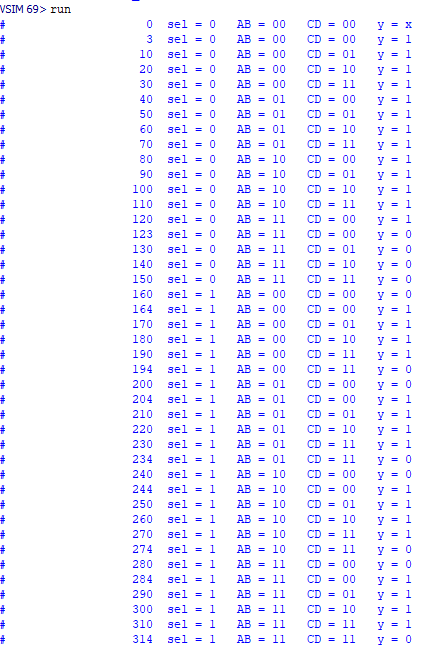
1. **测试模块**



1. **测试波形图：**



1. **显示输出（可选）：**

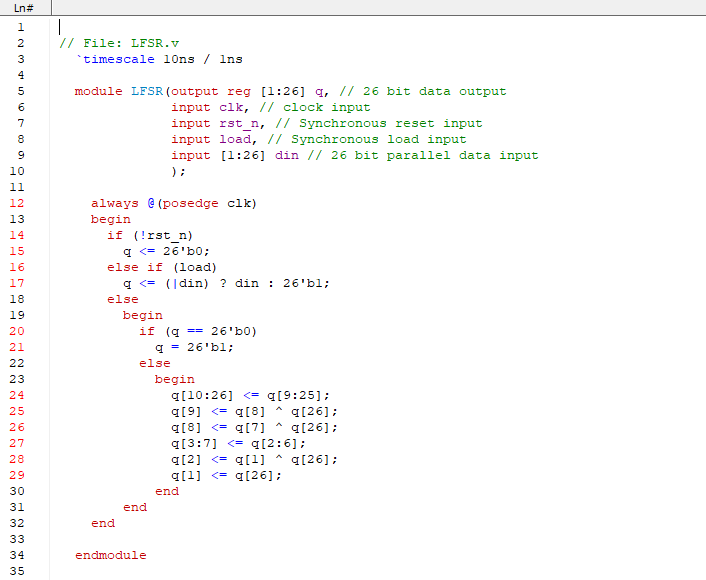


1. **设计说明：**

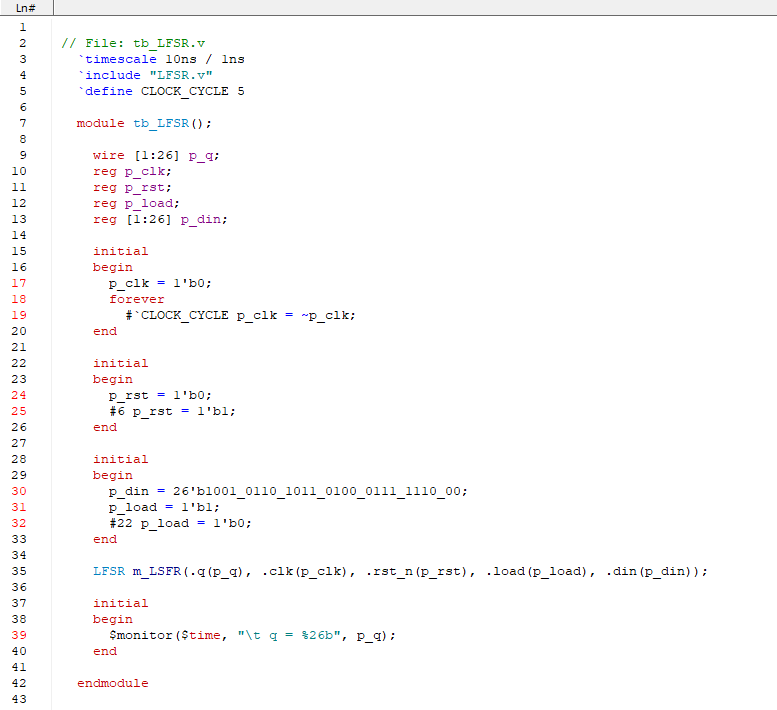
**先用两个nand门得到in0、in1，再用bufif0、bufif1完成2x1多路复用器。**

**第9题：**

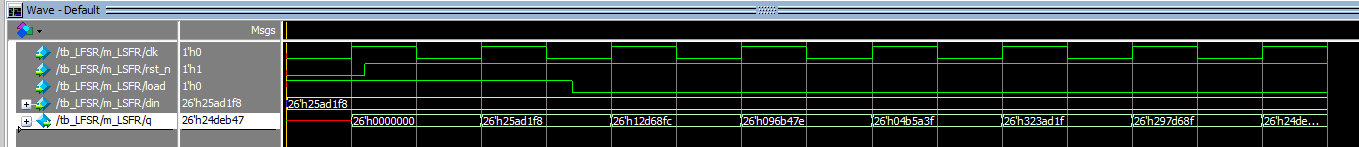
1. **设计模块**



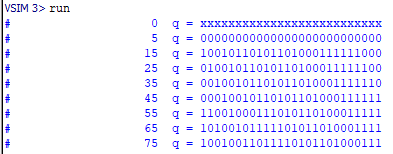
1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

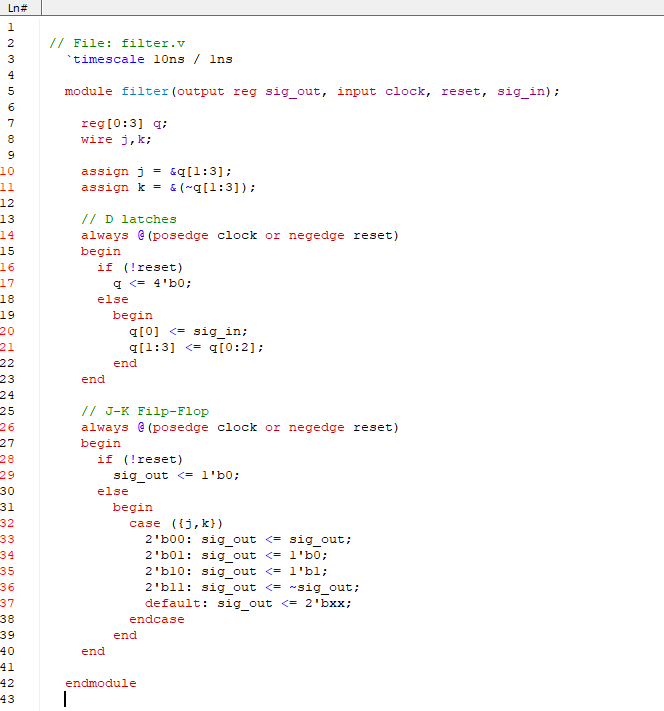


1. **设计说明：**

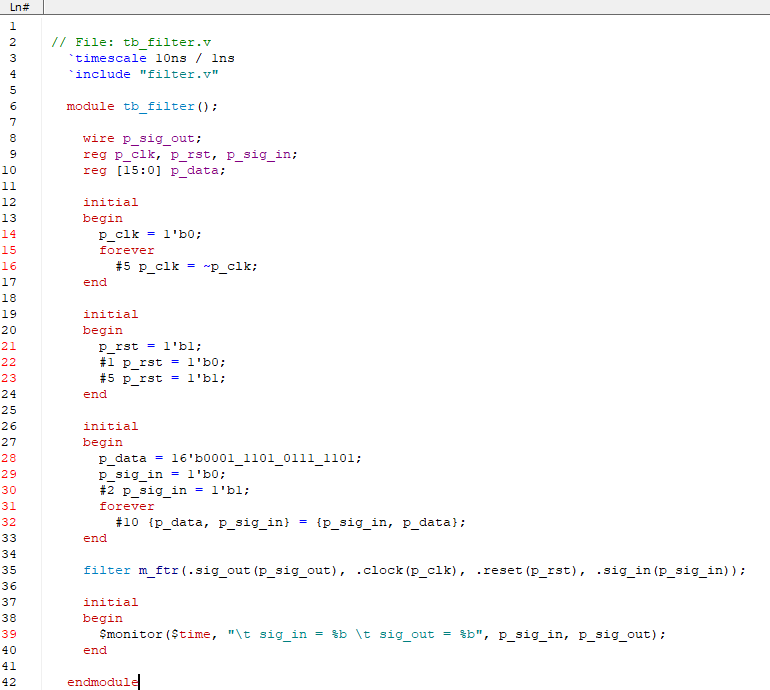
**根据LFSR的定义，依次按位移位或者进行异或操作。**

**第10题：**

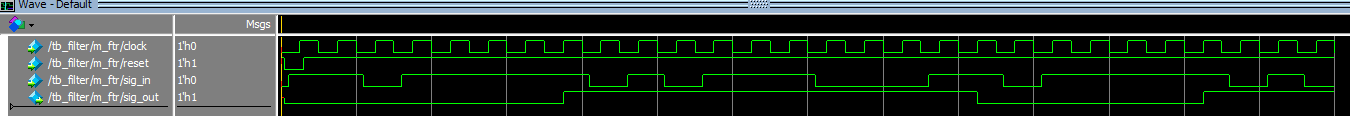
1. **设计模块**



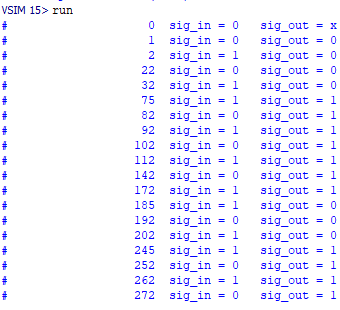
1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

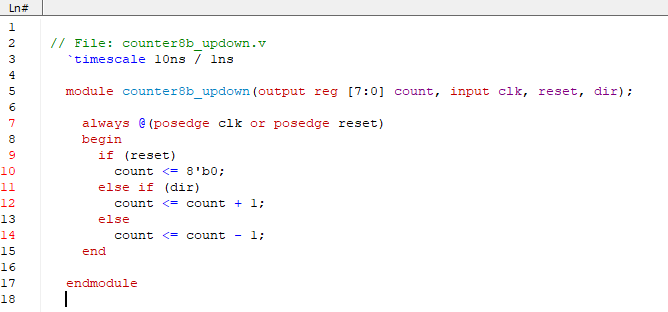


1. **设计说明：**

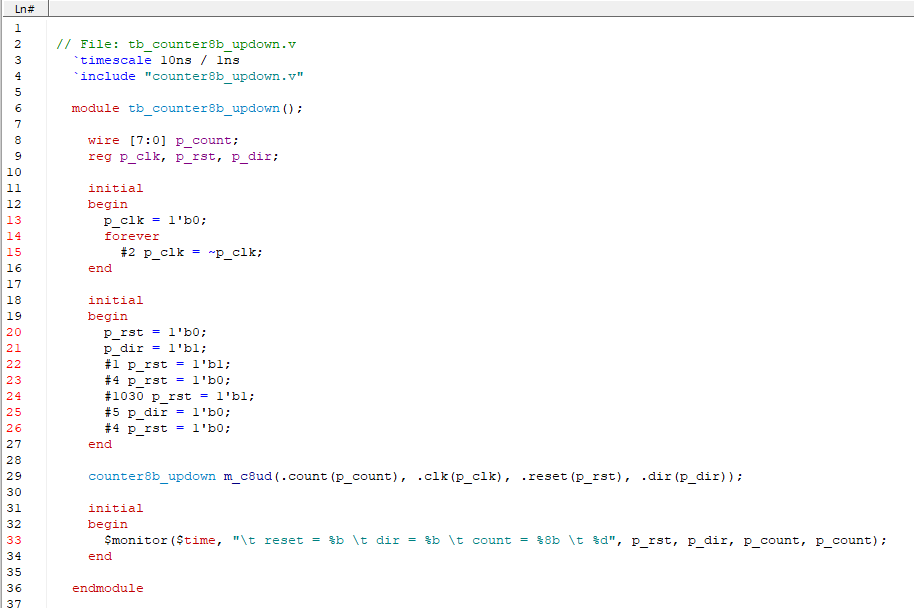
**本模块主要由一个D Latch和一个J-K FF组成，根据其真值表设计模块即可。**

**第11题：**

1. **设计模块**

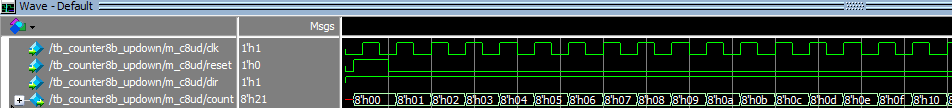


1. **测试模块**

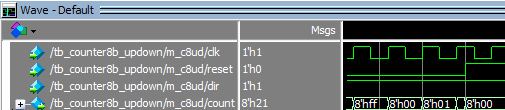


1. **测试波形图：**

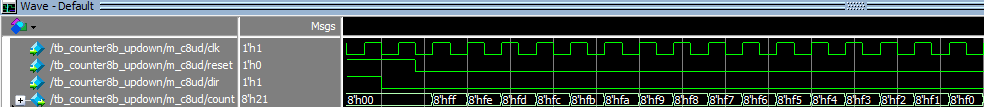
**开始计数（递增）：**



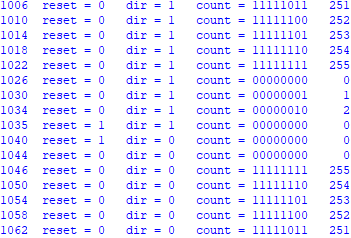
**Reset，从0开始：**



**Dir为0，递减计数：**



1. **显示输出：**

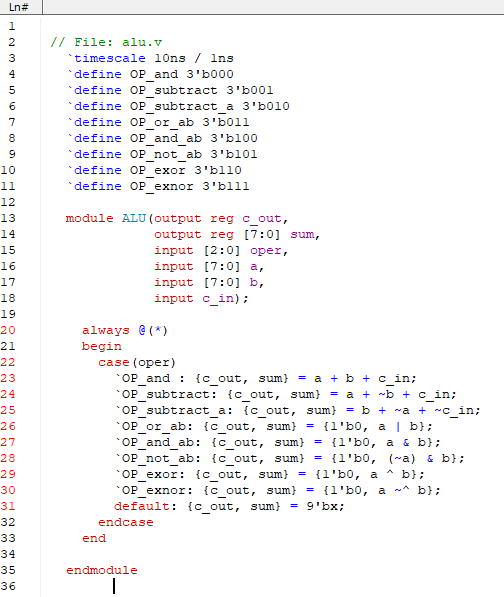


1. **设计说明：**

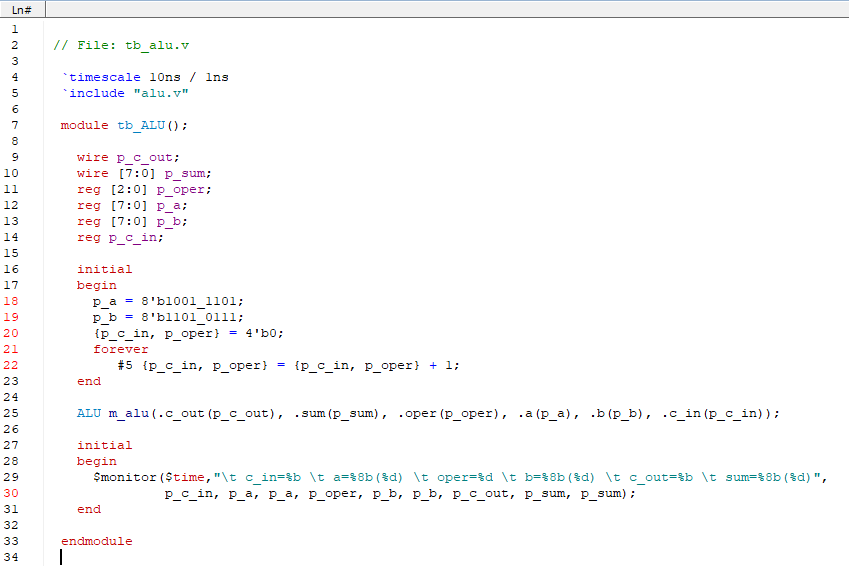
**采用异步复位，即always @(posedge clock or posedge reset)。**

**第12题：**

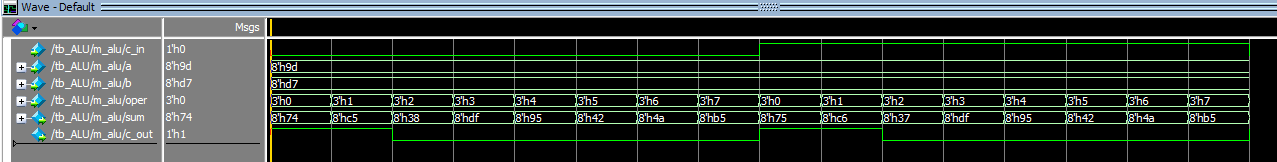
1. **设计模块**



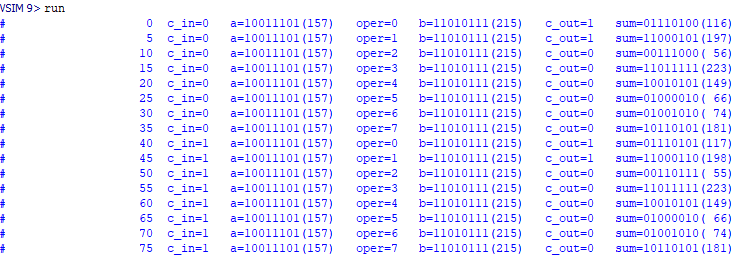
1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

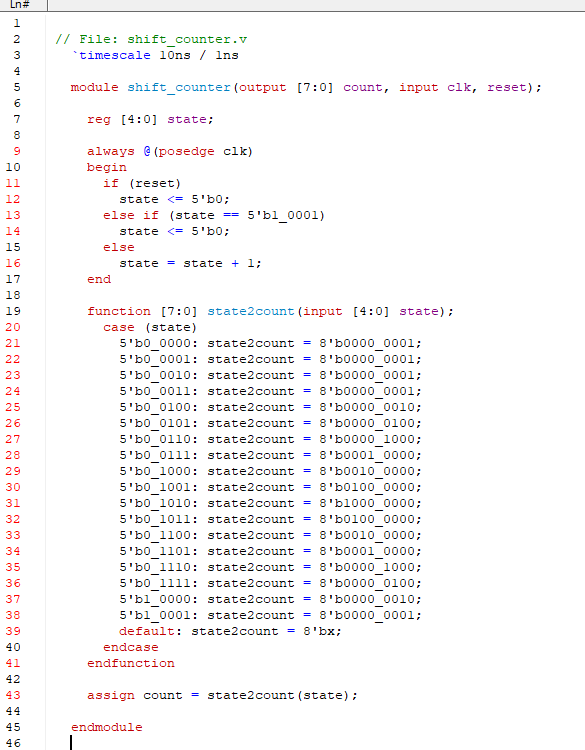


1. **设计说明：**

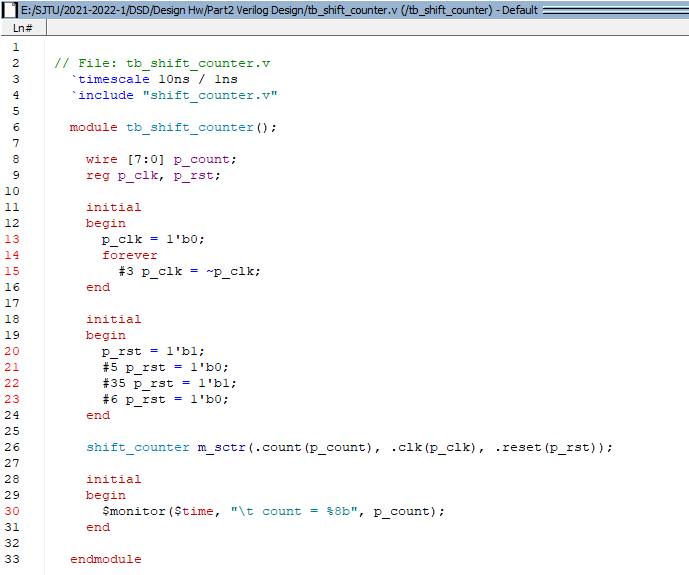
**根据功能表，按照case执行即可。**

**第13题：**

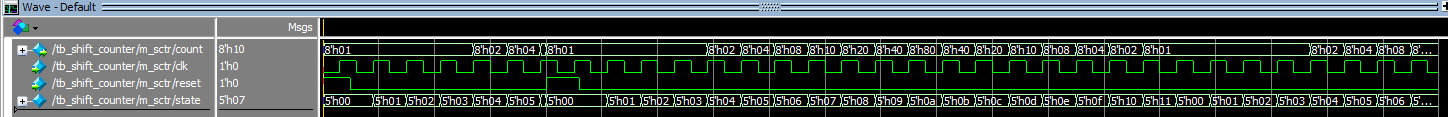
1. **设计模块**



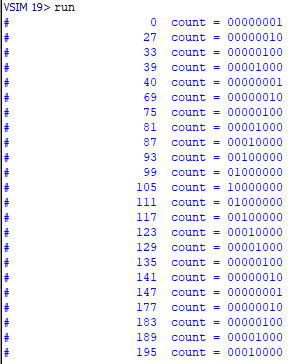
1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

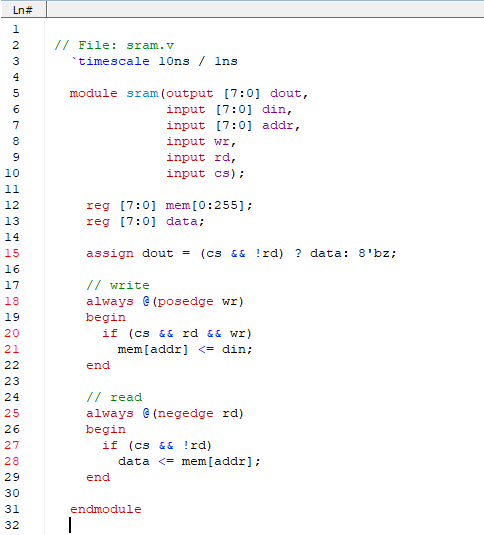


1. **设计说明：**

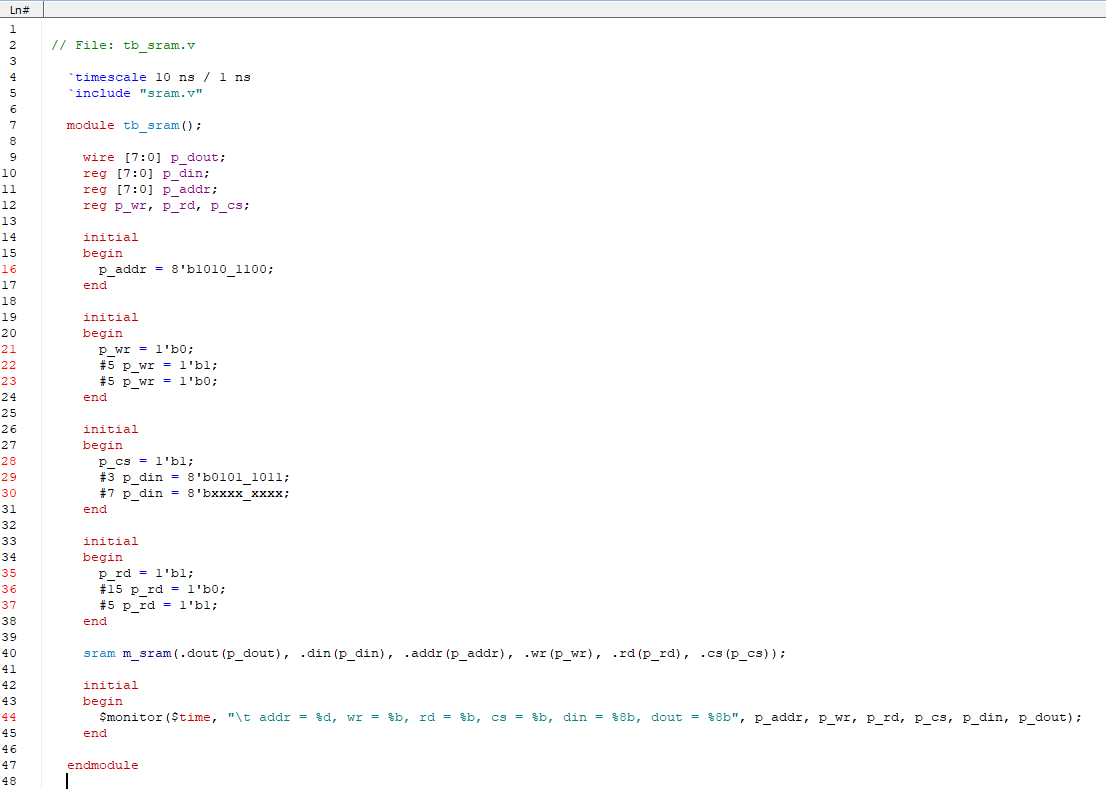
**根据题给出的计数模式，设计一个state2count函数，根据不同的state(reg [4:0])来确定相应的count。**

**第14题：**

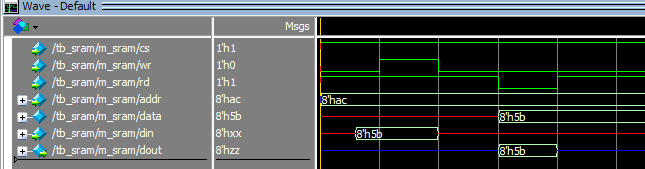
1. **设计模块**



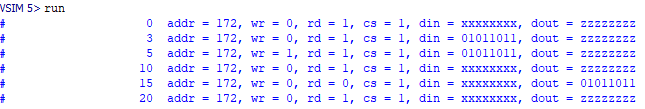
1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

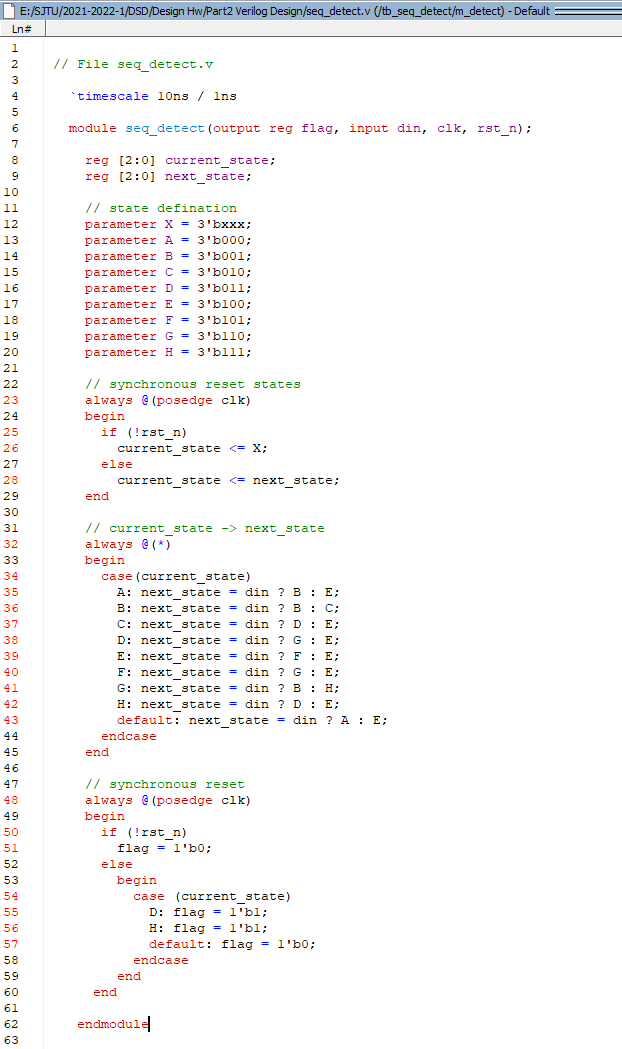


1. **设计说明：**

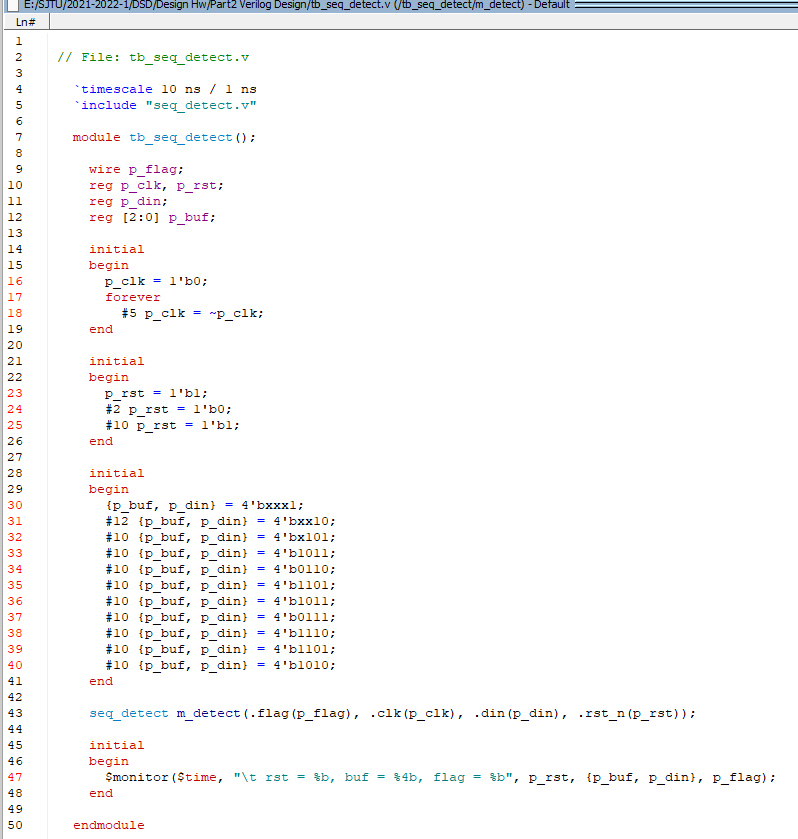
**根据不同情形设置输入和输出模式，使用data作为中间变量，将数据从mem[addr]中写入或读出。**

**第15题：**

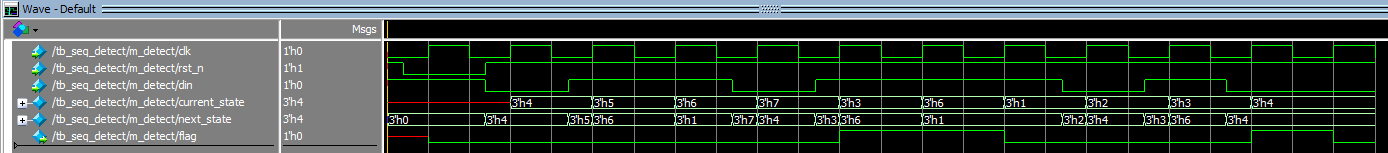
1. **设计模块**



1. **测试模块**



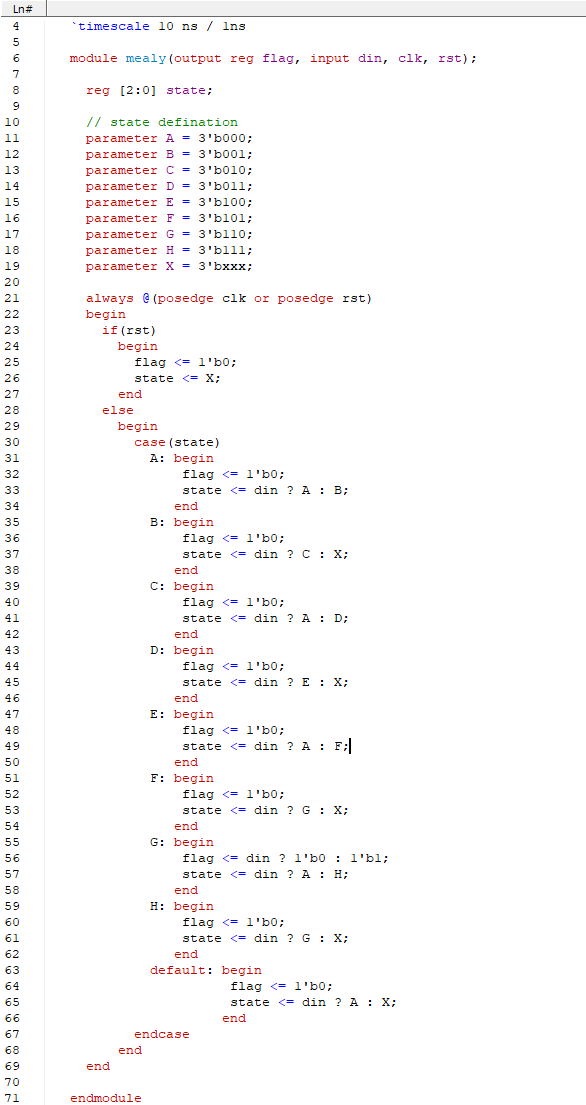
1. **测试波形图：**



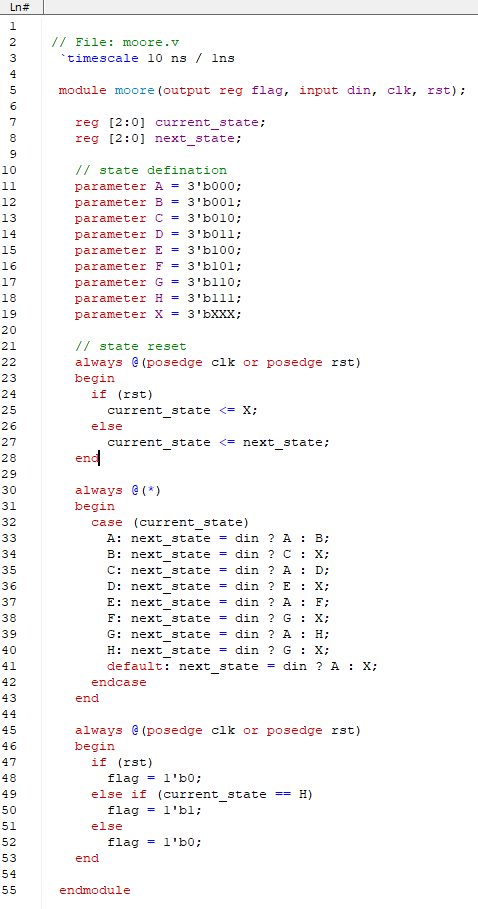
**第16题：**

1. **设计模块**

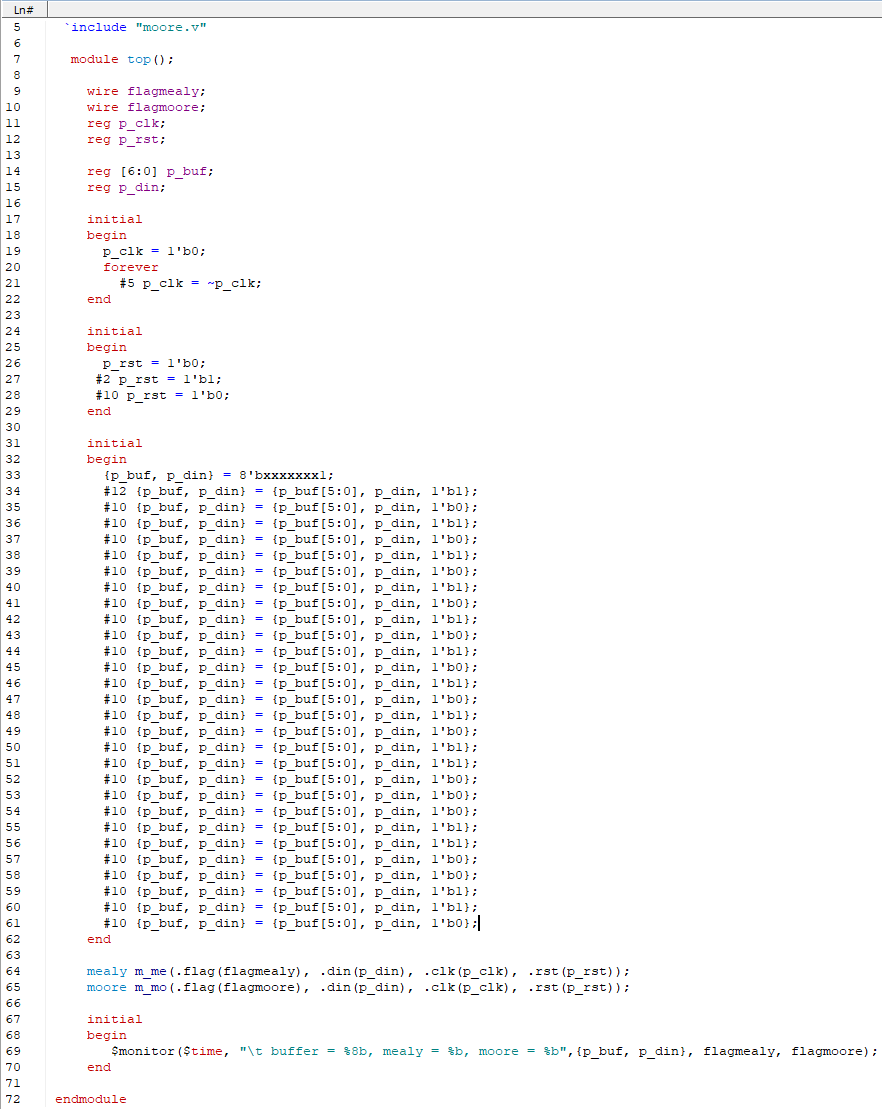
**mealy.v**



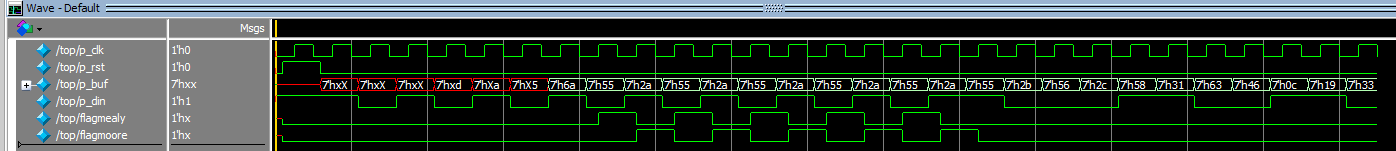
**moore.v**



1. **测试模块**



1. **测试波形图：**



1. **显示输出：**

